Grade 12 A/L ICT · Lesson 2

2.3 Von Neumann Architecture: Stored Program, CPU and the Fetch–Execute Cycle

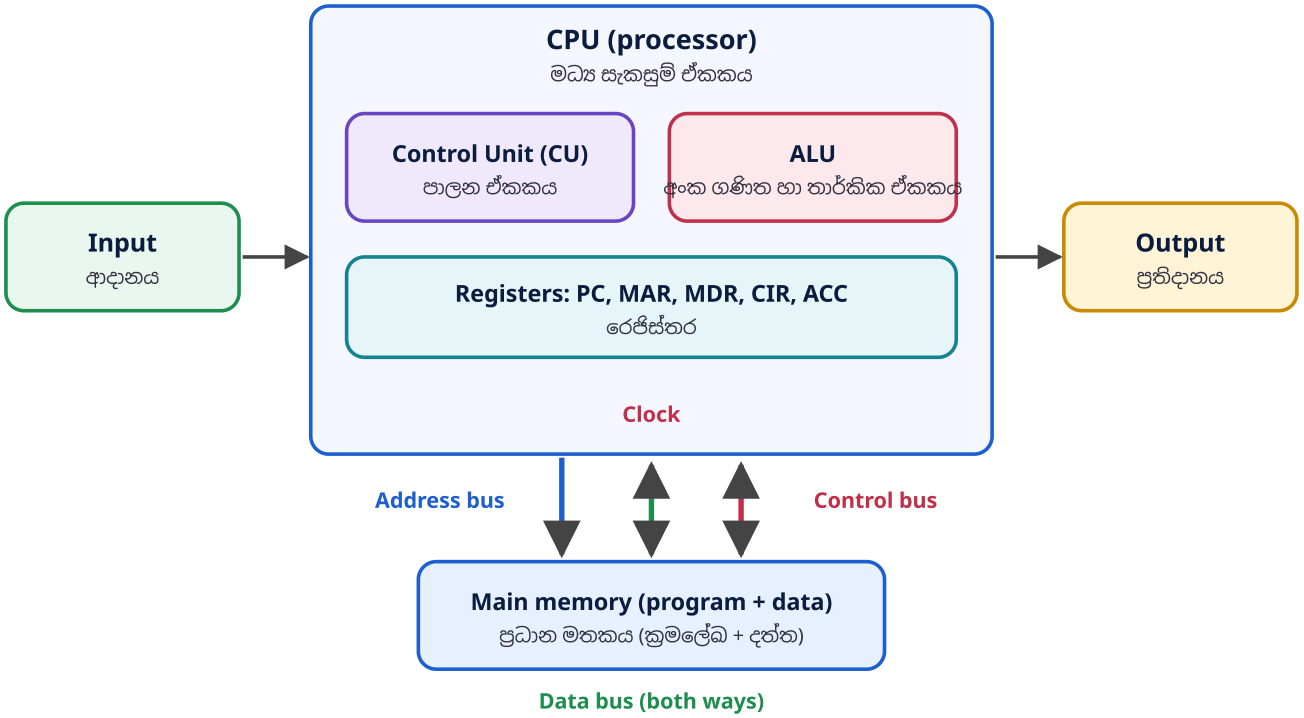
Syllabus 2.3. Almost every computer today follows one simple plan described by **John von Neumann** in 1945: keep the **program and the data together in the same memory**, and let the **CPU** fetch and run the instructions one by one. In this part you learn the **stored program concept**, the **components** of the model and how to draw it, the **fetch–execute cycle**, the jobs of the **ALU, CU, registers and buses**, and why we now use **multi-core processors**.

1. The stored program concept

Early machines such as ENIAC were programmed by **changing wires and switches** – a new job could take days. Von Neumann's idea (in his 1945 report on **EDVAC**) was: store the **instructions as numbers in memory**, exactly like data. To change the job, you just **load a different program** into memory.

- Program instructions and data are stored **together in the same main memory**.
- Every memory location has an **address**; the CPU reads and writes using addresses.
- Instructions are run **one after another (sequentially)** unless a jump instruction changes the order.

2. Components of the von Neumann model



The von Neumann architecture – learn to draw this.

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Input unit
Brings data and programs into the computer.

Memory unit
Holds both the program and the data.

Control unit (CU)
Fetches and decodes instructions and sends control signals.

Arithmetic and logic unit (ALU)
Does the calculations and comparisons.

Output unit
Sends results out to the user.

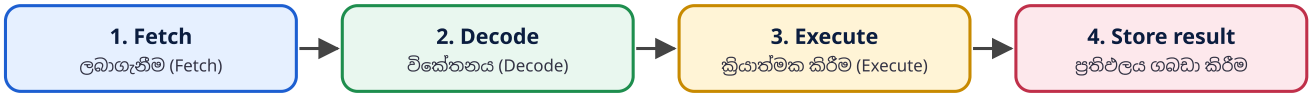
💡 When you draw the model in the exam: put the **CU and ALU (with registers) inside one CPU box**, show **memory** beside it, **input** and **output** at the sides, and label the arrows **data**, **address** and **control**.

3. Inside the CPU

Part	Job
ALU	Arithmetic (+, −, ×, ÷) and logic (AND, OR, NOT, comparing >, <, =)
Control unit (CU)	Fetches and decodes instructions, controls the timing with the clock, and directs data between parts
Registers	Tiny, very fast memory cells inside the CPU
Clock	Sends regular pulses; each pulse is one cycle

Register	What it holds
Program counter (PC)	The address of the next instruction
Memory address register (MAR)	The address to read from or write to
Memory data register (MDR / MBR)	The data or instruction just read, or about to be written
Current instruction register (CIR / IR)	The instruction being decoded and run
Accumulator (ACC)	The result from the ALU

4. The fetch–execute cycle



The CPU repeats this cycle billions of times each second.

- **Fetch:** PC → MAR; the instruction at that address comes to the MDR, then to the CIR; PC = PC + 1.
- **Decode:** the CU works out what the instruction means (the operation and the data it needs).

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- **Execute:** the CU sends signals; the ALU calculates, or data is moved, or a jump changes the PC.
- **Store:** the result is saved in the accumulator, a register or memory. Then the cycle starts again.

🧱 **Worked example: A CPU clock runs at 3.2 GHz. How long is one clock cycle?**
Cycle time = 1 ÷ frequency = 1 ÷ (3.2×10^9) s = **0.3125 ns**.

🧱 **Worked example: The same CPU needs on average 4 cycles per instruction. How many million instructions per second (MIPS) can one core run? What about 4 cores working fully in parallel?**
3.2 GHz = 3,200 million cycles per second. 3,200 ÷ 4 = **800 MIPS** per core. 4 cores: 800 × 4 = **3,200 MIPS** (best case).

5. Buses

A **bus** is a set of parallel wires that carries signals between the CPU, memory and input/output. The **system bus** has three parts:

Bus	Carries	Direction
Address bus	Memory addresses chosen by the CPU	One way: CPU → memory
Data bus	Data and instructions	Two ways
Control bus	Signals such as read, write, clock, interrupt	Two ways

🧱 **Worked example: How many memory locations can a 16-bit and a 32-bit address bus reach?**
n address lines give 2^n addresses. 2^{16} = **65,536** locations (64 K). 2^{32} = **4,294,967,296** locations (4 G).

🧱 **Worked example: A CPU has a 64-bit data bus. How many bytes can it move in one transfer?**
64 bits ÷ 8 = **8 bytes** at a time. A wider data bus moves more data per cycle.

💡 **Von Neumann bottleneck:** instructions and data share one bus to memory, so the fast CPU often waits for the slower memory. Cache memory and wider buses help reduce this.

6. Multi-core processors

A **core** is a complete processing unit (its own CU, ALU and registers). A **multi-core processor** has two or more cores on **one chip** (dual-core, quad-core, octa-core).

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- **Why needed:** making one core faster by raising the clock speed creates too much **heat** and uses too much **power**. Adding cores gives more work per second without a hotter clock.
- **Multitasking:** different programs can run on different cores at the same time.
- **Limit:** the speed-up is real only if the software is written to use many cores (multi-threaded).

🚀 **Beyond the syllabus (2026 update)** *Not required for the exam – read for interest.* **GPUs, NPUs and hybrid cores.** In 2026 a phone or laptop chip is a **system on a chip** with CPU cores plus a **GPU** (thousands of small cores for graphics and AI) and an **NPU** (neural processing unit) rated at 40+ **TOPS** (trillion operations per second) for on-device AI. Many CPUs mix **performance (P) cores** for heavy work and **efficiency (E) cores** to save battery.

Key Words

Stored program concept – Instructions and data are kept together in the same memory.

Von Neumann architecture – A computer design with input, output, memory, CU and ALU sharing one memory for program and data.

ALU – The part of the CPU that does arithmetic and logic operations.

Control unit – The part of the CPU that fetches, decodes and controls the running of instructions.

Register – A tiny, very fast memory location inside the CPU.

Program counter – The register that holds the address of the next instruction.

Accumulator – The register that holds the result of the ALU.

Fetch–execute cycle – The repeated steps fetch, decode and execute that the CPU follows.

Address bus – One-way bus that carries memory addresses from the CPU.

Data bus – Two-way bus that carries data and instructions.

Control bus – Bus that carries control signals such as read, write and clock.

Clock speed – The number of cycles per second, measured in hertz (GHz).

Multi-core processor – A chip with two or more complete processing cores.

Von Neumann bottleneck – The CPU waiting for memory because program and data share one bus.

EDVAC – Early computer in whose 1945 report the stored program idea was described.

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Sample Q&A

1. What is the stored program concept?

> **Answer:** Program instructions are stored in main memory together with the data, so the CPU can fetch and run them one by one, and a new program can be loaded without rewiring.

2. Name the five main components of the von Neumann model.

> **Answer:** Input unit, output unit, memory unit, control unit (CU) and arithmetic and logic unit (ALU).

3. Describe the fetch stage of the cycle.

> **Answer:** The address in the PC is copied to the MAR; the instruction at that address is read into the MDR and copied to the CIR; the PC is increased by one.

4. Compare the address bus and the data bus.

> **Answer:** The address bus carries addresses one way from the CPU and its width decides how many locations can be reached. The data bus carries data both ways and its width decides how much is moved at once.

5. What does the ALU do? Give examples.

> **Answer:** It does arithmetic such as addition and subtraction and logic such as AND, OR, NOT and comparing two numbers.

6. Why are multi-core processors needed?

> **Answer:** Raising the clock speed makes too much heat and uses too much power, so more cores are added to do more work at the same time and to run many programs together.

MCQ

1. In the von Neumann architecture, programs and data are stored:

A. Only on the hard disk
B. Together in the same memory
C. In the output unit
D. In separate wires and switches
E. Only in the ALU

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2. Which register holds the address of the next instruction?

A. MDR
B. ALU
C. Program counter (PC)
D. Accumulator
E. CIR

3. Which bus is one-way only?

A. Data bus
B. All buses
C. USB bus
D. Address bus
E. Control bus

4. Comparing two numbers to see which is bigger is done by the:

A. Control bus
B. ALU
C. Program counter
D. MAR
E. Input unit

5. What is the cycle time of a 3.2 GHz clock?

A. 0.32 s
B. 3.2 ns
C. 1 ns
D. 312.5 ns
E. 0.3125 ns

6. A 16-bit address bus can address:

A. 256 locations
B. 4,294,967,296 locations
C. 16 locations
D. 32,768 locations
E. 65,536 locations

7. The correct order of the cycle is:

A. Fetch → decode → execute
B. Decode → fetch → execute
C. Fetch → execute → decode
D. Execute → fetch → decode
E. Store → decode → fetch

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8. The main reason for multi-core processors is:

A. Keyboards became faster
B. Hard disks need cores
C. Higher clock speeds cause too much heat and power use
D. Buses were removed
E. Memory became cheaper

9. A 64-bit data bus moves how many bytes at once?

A. 8
B. 64
C. 512
D. 16
E. 4

10. The von Neumann bottleneck happens because:

A. The CPU has too many cores
B. Program and data share one path to memory
C. Output is too fast
D. The ALU has no registers
E. There is no clock

11. Read and write signals travel on the:

A. Control bus
B. Program counter
C. Address bus
D. Output unit
E. Accumulator

12. A 3.2 GHz core needs 4 cycles per instruction. Its speed is:

A. 80 MIPS
B. 400 MIPS
C. 3,200 MIPS
D. 12.8 MIPS
E. 800 MIPS

13. Which term means: “Instructions and data are kept together in the same memory”?

A. Program counter
B. Fetch–execute cycle
C. Control bus
D. Stored program concept
E. ALU

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14. Which term means: “A computer design with input, output, memory, CU and ALU sharing one memory for program and data”?

A. Accumulator
B. Clock speed
C. Address bus
D. Von Neumann architecture
E. Control unit

15. Which term means: “The part of the CPU that does arithmetic and logic operations”?

A. Fetch–execute cycle
B. Data bus
C. ALU
D. Register
E. Multi-core processor

16. Which term means: “The part of the CPU that fetches, decodes and controls the running of instructions”?

A. Control unit
B. Von Neumann bottleneck
C. Program counter
D. Address bus
E. Control bus

17. Which term means: “A tiny, very fast memory location inside the CPU”?

A. Accumulator
B. Clock speed
C. Register
D. EDVAC
E. Data bus

18. Which term means: “The register that holds the address of the next instruction”?

A. Fetch–execute cycle
B. Stored program concept
C. Control bus
D. Program counter
E. Multi-core processor

19. Which term means: “The register that holds the result of the ALU”?

A. Von Neumann architecture
B. Accumulator
C. Address bus
D. Clock speed
E. Von Neumann bottleneck

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20. Which term means: “The repeated steps fetch, decode and execute that the CPU follows”?

A. Multi-core processor
B. EDVAC
C. Data bus
D. ALU
E. Fetch–execute cycle

Structured Questions

1. (a) State the stored program concept. (b) Why was it an improvement over ENIAC? *(3 marks)*

> (a) Instructions and data are stored together in main memory; instructions are fetched and run one by one; (b) ENIAC was rewired for each job, now a new program is simply loaded.

2. Draw a labelled diagram of the von Neumann architecture showing the buses. *(5 marks)*

> CPU box containing CU, ALU and registers; memory unit; input unit; output unit; address, data and control buses labelled with correct directions.

3. Explain the fetch–execute cycle using PC, MAR, MDR and CIR. *(5 marks)*

> PC copied to MAR; instruction read into MDR; copied to CIR and PC increased; CU decodes the instruction; ALU or CU executes it and the result is stored.

4. A computer has a 32-bit address bus and a 64-bit data bus. (a) How many locations can it address? (b) How many bytes move in one transfer? *(2 marks)*

> (a) 2^{32} = 4,294,967,296 locations; (b) 64 ÷ 8 = 8 bytes.

5. (a) What is a multi-core processor? (b) Give two advantages and one limitation. *(4 marks)*

> (a) A chip with two or more complete cores; (b) more work at the same time without a hotter clock; better multitasking; limitation: software must be multi-threaded to benefit.

Summary

- Stored program concept: program and data together in one memory (von Neumann, 1945, EDVAC).
- Components: input, output, memory, control unit and ALU.
- The CPU repeats fetch → decode → execute → store using PC, MAR, MDR, CIR and ACC.
- The address bus is one-way; data and control buses are two-way.
- n address lines reach 2^n locations; a 64-bit data bus moves 8 bytes at once.
- Multi-core chips give more work per second without too much heat.

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MCQ answer key – 2.3

1. **B** – Stored program concept.
2. **C** – PC points to the next instruction.
3. **D** – CPU → memory.
4. **B** – A logic operation.
5. **E** – 1 ÷ 3.2 = 0.3125 ns.
6. **E** – 2^{16} = 65,536.
7. **A** – Fetch first, then decode, then execute.
8. **C** – Heat and power limit.
9. **A** – 64 ÷ 8 = 8.
10. **B** – CPU waits for memory.
11. **A** – Control signals.
12. **E** – 3,200 ÷ 4 = 800.
13. **D** – Stored program concept – Instructions and data are kept together in the same memory.
14. **D** – Von Neumann architecture – A computer design with input, output, memory, CU and ALU sharing one memory for program and data.
15. **C** – ALU – The part of the CPU that does arithmetic and logic operations.
16. **A** – Control unit – The part of the CPU that fetches, decodes and controls the running of instructions.
17. **C** – Register – A tiny, very fast memory location inside the CPU.
18. **D** – Program counter – The register that holds the address of the next instruction.
19. **B** – Accumulator – The register that holds the result of the ALU.
20. **E** – Fetch–execute cycle – The repeated steps fetch, decode and execute that the CPU follows.

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