Grade 12 A/L ICT · Lesson 4

Lesson 4 A/L Exam Practice: Questions and Answers

This practice paper assesses **Lesson 4: Fundamentals of Digital Circuits** (syllabus competency 4). Paper I has 30 five-option MCQs. Paper II Part A has four structured questions; Part B has three essays. Marking points are shown in brackets.

Paper I – Multiple choice questions (30)

1. Which gate outputs 1 only when all inputs are 1?

A. NOR
B. AND
C. OR
D. XOR
E. NOT

2. NOT of 0 is

A. 0
B. undefined
C. 1
D. A
E. 2

3. XOR of 1 and 1 is

A. undefined
B. 2
C. carry 1 only
D. 0
E. 1

4. NAND equals

A. A + B
B. $(A \cdot B)'$
C. $A \cdot B$
D. $(A + B)'$
E. $A \oplus B$

© 2026 schoolict.net (Ruwan Mangala Suraweera) · All rights reserved

5. Universal gates are

A. AND and OR
B. AND and XOR
C. NOT only
D. XOR and XNOR
E. NAND and NOR

6. A 3-input truth table has

A. 4
B. 8 rows
C. 6
D. 3
E. 9

7. XNOR is 1 when inputs are

A. different
B. floating
C. both 1 only
D. equal
E. both 0 only

8. NOR of 0 and 0 is

A. B
B. A
C. undefined
D. 0
E. 1

9. A NAND A equals

A. A
B. A′
C. 0
D. A · A
E. 1

10. De Morgan: (A + B)′ =

A. A′ + B′
B. A′
C. A · B
D. A′ · B′
E. A + B

© 2026 schoolict.net (Ruwan Mangala Suraweera) · All rights reserved

11. SOP means

A. Single Output Path
B. Sum of Powers
C. Sum of Products
D. Product of Sums
E. Signed OR Product

12. $A \cdot B + A \cdot B'$ simplifies to

A. 0
B. $A + B$
C. $A \cdot B$
D. B
E. A

13. Allowed K-map group sizes

A. Only 5
B. Only 3
C. Any odd
D. 1, 2, 4, 8
E. 3, 5

14. POS means

A. Product of Sums
B. Sum of Products
C. Product of Squares
D. Positive OR Sum
E. Parallel Output Set

15. $A + A' =$

A. A'
B. A
C. 1
D. $A \cdot A'$
E. 0

16. $F = \Sigma m(1,2,3)$ for 2 vars →

A. 0
B. B'
C. $A \cdot B$
D. A'
E. $A + B$

© 2026 schoolict.net (Ruwan Mangala Suraweera) · All rights reserved

17. Design starts with

A. identifying the need
B. skipping the table
C. POS only
D. drawing random gates
E. buying chips

18. Door alarm F = D · N uses

A. NOR
B. XOR
C. OR
D. NOT
E. AND

19. Majority of A,B,C is

A. AB + BC + AC
B. A′ + B′ + C′
C. A · B · C
D. A ⊕ B ⊕ C
E. A + B + C

20. · maps to which gate?

A. AND
B. NOR
C. NOT
D. OR
E. XOR

21. F = E · S′ needs

A. XOR only
B. NOT and AND
C. OR only
D. two OR gates
E. NAND only

22. Max inputs in syllabus designs

A. 5
B. 1
C. 16
D. 3
E. 8

© 2026 schoolict.net (Ruwan Mangala Suraweera) · All rights reserved

23. + maps to which gate?

A. AND
B. XOR
C. NOT
D. NAND
E. OR

24. Half-adder Sum is

A. A ⊕ B
B. A + B
C. A · B
D. majority
E. A ⊕ B ⊕ Cin

25. Half-adder Carry is

A. A′
B. A · B
C. Cin
D. A + B
E. A ⊕ B

26. Full adder inputs are

A. S, C
B. A only
C. A, B, Cin
D. Q, Q′
E. A, B only

27. Full-adder S equals

A. A ⊕ B ⊕ Cin
B. AB + BC + AC
C. A + B
D. A · B
E. A ⊕ B

28. A flip-flop stores

A. 0 bits
B. an instruction
C. 8 bits always
D. 1 bit
E. 1 byte

© 2026 schoolict.net (Ruwan Mangala Suraweera) · All rights reserved

29. SR with S=R=0

A. is forbidden
B. clears Cin
C. holds previous Q
D. resets Q
E. sets Q

30. Forbidden SR input is

A. S=1, R=0
B. S=0, R=0
C. S=1, R=1
D. Q=0
E. S=0, R=1

© 2026 schoolict.net (Ruwan Mangala Suraweera) · All rights reserved

Paper II Part A – Structured questions

1. Logic gates and truth tables *(8 marks)*

(i) Define a logic gate and state how many rows a 2-input truth table has. *(2 marks)*
(ii) Write truth tables for AND and XOR. *(4 marks)*
(iii) Why are NAND and NOR called universal? Show NOT from NAND. *(2 marks)*

2. Boolean algebra and K-maps *(8 marks)*

(i) State De Morgan’s laws. *(2 marks)*
(ii) Simplify A·B + A·B′ and A + A′·B. *(2 marks)*
(iii) Using a K-map idea, simplify F=Σm(1,2,3) for two variables. *(2 marks)*
(iv) Distinguish SOP and POS. *(2 marks)*

3. Circuit design *(8 marks)*

(i) List the four design steps. *(2 marks)*
(ii) Design a night door alarm: table and expression. *(3 marks)*
(iii) Write the majority function and evaluate ABC=110 and 100. *(3 marks)*

4. Adders and flip-flops *(8 marks)*

(i) Give S and C for a half adder and complete the row A=1,B=1. *(3 marks)*
(ii) Give S and Cout for a full adder. Find them for A=1,B=0,Cin=1. *(3 marks)*
(iii) Explain how a flip-flop stores a bit and the meaning of S=R=0. *(2 marks)*

© 2026 schoolict.net (Ruwan Mangala Suraweera) · All rights reserved

Paper II Part B – Essay questions

1. Gates and Boolean simplification *(10 marks)*

(i) Explain NOT, AND, OR and XOR with one everyday sentence each and their truth-table idea. *(4 marks)*
(ii) Why simplify Boolean expressions? Simplify A·B + A·B′ showing laws. *(3 marks)*
(iii) Describe how a K-map helps, including allowed group sizes. *(3 marks)*

2. Designing a useful circuit *(10 marks)*

(i) Choose a real Sri Lankan school or home need that fits three inputs. Name inputs and output. *(3 marks)*
(ii) Write the truth table (8 rows) for your need and the SOP expression before simplifying. *(4 marks)*
(iii) Simplify if possible and list the gates in the final circuit. *(3 marks)*

3. Adders, ALU and memory cells *(11 marks)*

(i) Compare the half adder and the full adder (inputs, outputs, expressions, use). *(5 marks)*
(ii) Explain how flip-flops use feedback to store bits and how registers relate to them. *(4 marks)*
(iii) State one reason S=R=1 is avoided in a basic SR latch. *(2 marks)*

© 2026 schoolict.net (Ruwan Mangala Suraweera) · All rights reserved

Exam tips

- Learn all seven gate truth tables until you can write them in under a minute.
- Universal-gate questions almost always want A NAND A = NOT A.
- Write the law name beside every Boolean simplification line.
- K-map groups are only 1, 2, 4, 8 – never circle three 1s.
- Design answers score when inputs/outputs are named in words and in letters.
- Half adder = XOR + AND; full adder adds Cin and uses majority for Cout.
- Remember SR: 10 set, 01 reset, 00 hold, 11 forbidden.
- In Paper I, watch for NOT / NAND / NOR wording traps.
- In Paper II, one mark ≈ one clear point or one correct table row.
- Draw gate circles for inversion – examiners look for the bubble.
- Check arithmetic examples: 1+1 = 10_2 means S=0, C=1.
- Beyond boxes (FPGA, CMOS counts) are for interest – exam tests the syllabus only.

© 2026 schoolict.net (Ruwan Mangala Suraweera) · All rights reserved

Answers and explanations

Paper I

1. **B** – AND needs every input = 1.
2. **C** – Inverter flips 0 to 1.
3. **D** – Same inputs → XOR = 0.
4. **B** – NOT of AND.
5. **E** – Each alone can build every gate.
6. **B** – $2^3 = 8$.
7. **D** – Equality gate.
8. **E** – NOR = 1 only for 00.
9. **B** – Tied NAND = NOT.
10. **D** – Break bar, change + to ·.
11. **C** – OR of AND terms.
12. **E** – A(B+B′)=A.
13. **D** – Powers of two.
14. **A** – AND of OR terms.
15. **C** – Complement law.
16. **E** – K-map gives A + B.
17. **A** – Need first.
18. **E** – Both conditions required.
19. **A** – At least two 1s.
20. **A** – . is AND.
21. **B** – Invert S, AND with E.
22. **D** – Up to three.
23. **E** – + is OR.
24. **A** – XOR.
25. **B** – AND.
26. **C** – Includes carry-in.
27. **A** – Triple XOR.
28. **D** – One-bit memory cell.
29. **C** – Hold / memory.
30. **C** – Both active.

© 2026 schoolict.net (Ruwan Mangala Suraweera) · All rights reserved

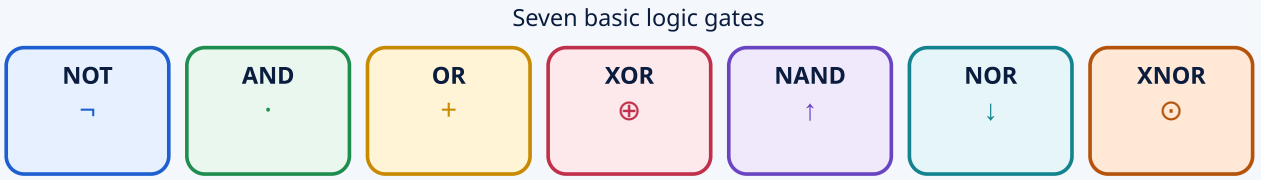
Paper II Part A – model answers and marking points

1. *(8 marks)*

(i) (2 marks)
Circuit with binary in/out (1); 4 rows (1).

(ii) (4 marks)
AND: 00,01,10 → 0; 11 → 1 (2); XOR: 00,11 → 0; 01,10 → 1 (2).

(iii) (2 marks)
Can build any gate alone (1); A NAND A = A′ (1).



Seven basic logic gates.

🎯 Examiner tip: always write every row of a truth table – missing a row loses marks.

© 2026 schoolict.net (Ruwan Mangala Suraweera) · All rights reserved

2. *(8 marks)*

(i) (2 marks)
$(A \cdot B)' = A' + B'$ (1); $(A + B)' = A' \cdot B'$ (1).

(ii) (2 marks)
A (1); A + B (1).

(iii) (2 marks)
Groups give A and B (1); F = A + B (1).

2-variable Karnaugh map

A \ B	0	1
0	m0	m1
1	m2	m3

Group adjacent 1s to simplify

2-variable K-map.

(iv) (2 marks)
SOP = OR of products / minterms for F=1 (1); POS = AND of sums / maxterms for F=0 (1).

🎯 Examiner tip: show the law you use at each simplification step.

© 2026 schoolict.net (Ruwan Mangala Suraweera) · All rights reserved

3. *(8 marks)*

(i) (2 marks)
Need; truth table; expression (+simplify); draw gates (½ each, round to 2).

(ii) (3 marks)
DN 00,01,10 → 0; 11 → 1 (2); F=D·N (1).



Design flow.

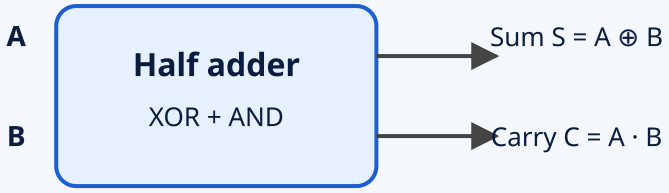
(iii) (3 marks)
F=AB+BC+AC (1); 110 → 1 (1); 100 → 0 (1).

🎯 Examiner tip: label every input and output on your circuit diagram.

© 2026 schoolict.net (Ruwan Mangala Suraweera) · All rights reserved

4. *(8 marks)*

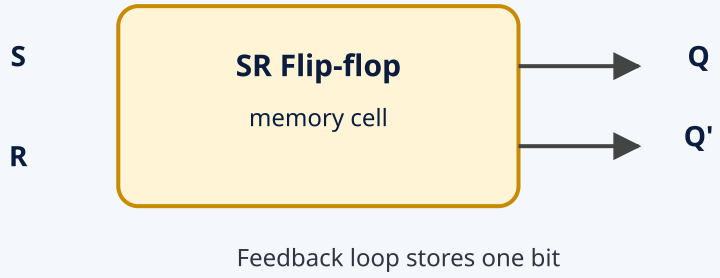
(i) (3 marks)
S=A⊕B, C=A·B (2); S=0,C=1 (1).



Half adder.

(ii) (3 marks)
S=A⊕B⊕Cin, Cout=majority (2); S=0, Cout=1 (1).

(iii) (2 marks)
Feedback holds one bit (1); S=R=0 holds previous Q (1).



SR flip-flop.

🎯 Examiner tip: never write S=R=1 as a valid SR latch state.

© 2026 schoolict.net (Ruwan Mangala Suraweera) · All rights reserved

Paper II Part B – model answers and marking points

1. *(10 marks)*

> **(i)** (4 marks)
> NOT flips (1); AND all must be true (1); OR any true (1); XOR different (1).

> **(ii)** (3 marks)
> Fewer gates / cost / speed (1); $A(B+B')=A\cdot 1=A$ (2).

> **(iii)** (3 marks)
> Adjacent 1s differ by one bit (1); groups 1,2,4,8 (1); each group → product term (1).

🎯 Examiner tip: link every law name to the algebraic line you write.

2. *(10 marks)*

> **(i)** (3 marks)
> Clear need (1); three named binary inputs (1); one named output (1).

> **(ii)** (4 marks)
> Correct 8 rows matching the need (3); SOP from F=1 rows (1).

> **(iii)** (3 marks)
> Valid simplification or state already minimal (1); gate list $\cdot \rightarrow$ AND $+ \rightarrow$ OR $' \rightarrow$ NOT (2).

🎯 Examiner tip: invent a need you can explain in one sentence – markers reward clarity.

3. *(11 marks)*

> **(i)** (5 marks)
> HA: A,B → $S=A\oplus B$, $C=A\cdot B$; LSB only (2); FA: +Cin → $S=A\oplus B\oplus Cin$, Cout=majority; multi-bit chain (2); both in ALU (1).

> **(ii)** (4 marks)
> Feedback holds state / 1 bit (2); SR hold when S=R=0 (1); register = group of flip-flops (1).

> **(iii)** (2 marks)
> Outputs fight / undefined next state (2).

🎯 Examiner tip: draw the HA/FA block even if the question does not demand a perfect symbol.

© 2026 schoolict.net (Ruwan Mangala Suraweera). All rights reserved.